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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/893,791	06/29/2001	Yutaka Kobayashi	PNDF-01068	4575

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EXAMINER	
CHU, CHRIS C	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/893,791	KOBAYASHI, YUTAKA	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for R ply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 4 and 16 - 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 4 and 16 - 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on June 5, 2003 has been received and entered in the case.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "102" and "15 or 46" have both been used to designate conductor wiring. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art of Fig. 1 in view of Takenaka et al.

Regarding claim 1, the acknowledged prior art discloses in Fig. 1 a semiconductor device, comprising:

- a semiconductor chip (100);
- a chip-mounting substrate (103) which is provided with the semiconductor chip mounted on a top surface thereof and first conductive pads (107) formed on a bottom surface thereof and connected with the semiconductor chip electrically;
- solder balls (106) formed on the first conductive pads;
- a printed circuit board (104) on which second conductive pads (108) connected with the solder balls are formed; and
- underfill material (105) injected into a clearance formed between the chip-mounting substrate and the printed circuit board,

The acknowledged prior art does not disclose a solder mask formed on a bottom surface of said chip-mounting substrate, said solder mask having an uneven roughness, wherein said

uneven roughness is formed on a surface which is brought into contact with said material of said printed circuit board, wherein said uneven roughness exists on said bottom surface of the chip-mounting substrate and wherein the uneven roughness on said bottom surface increases an area of a contact surface. However, Takenaka et al. teaches in Fig. 12, Fig. 14 and column 3, line 66 ~ 68 a solder mask (85) formed on a bottom surface of a chip-mounting substrate (45), said solder mask having an uneven roughness, wherein said uneven roughness is formed on a surface which is brought into contact with a material of a printed circuit board (21), wherein the uneven roughness exists on a bottom surface (10b) of the chip-mounting substrate (10) and wherein the uneven roughness on said bottom surface increases an area of a contact surface between the chip-mounting substrate and the underfill material. It would have been obvious to one of ordinary skill in the art at the time of the present invention was made to use the uneven rough surface of Takenaka et al. in the device of the acknowledged prior art of Fig. 1 in order to increase adhesion strength as taught by Takenaka et al. in column 2, lines 9 ~ 12.

Regarding claim 3, Takenaka et al. discloses in Fig. 5 the uneven roughness being shaped into at least one of a slit-like configuration and a dimple-like configuration.

Regarding claim 21, Takenaka et al. discloses in Fig. 12, Fig. 14 and column 3, line 66 ~ 68 said uneven roughness being continuously formed on said solder mask.

6. Claims 2 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art of Fig. 1 in view of Takenaka et al. as applied to claim 1 above, and further in view of Enomoto et al.

Regarding claim 2, the acknowledged prior art of Fig. 1 and Takenaka et al. disclose a claimed invention except for the uneven roughness being formed on at least one of the first conductive pads and the second conductive pads selectively. However, Enomoto et al. discloses in Fig. 1d an uneven roughness being formed on an second conductive pads (6). It would have been obvious to one of ordinary skill in the art at the time of the present invention was made to use the uneven roughness of Enomoto et al. in the device of the acknowledged prior art of Fig. 1 and Takenaka et al. in order to provide an adhesive for the printed circuit board having excellent thermal resistance, electrical resistance, chemical stability and adhesion property to the printed circuit board as taught by Enomoto et al. in column 2, lines 43 ~ 48.

Regarding claim 16, Enomoto et al. discloses in Fig. 1d the printed circuit board having a dimple-like shaped configuration.

7. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art of Fig. 1 in view of Takenaka et al. as applied to claim 1 above, and further in view of Kaskoun et al.

The acknowledged prior art of Fig. 1 and Takenaka et al. disclose a claimed invention except for a surface of said chip-mounting substrate having a slit-like shaped configuration. However, Kaskoun et al. discloses in Fig. 1 a surface of said chip-mounting substrate (13) having a slit-like shaped configuration. It would have been obvious to one of ordinary skill in the art at the time of the present invention was made to use the slit-like shaped configuration of Kaskoun et al. in the device of the acknowledged prior art of Fig. 1 and Takenaka et al. in order to

decrease tacking pressure during the assembly process as taught by Kaskoun et al. in column 3, lines 62 ~ 63.

8. Claims 4, 18, 19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kweon et al. in view of Takada et al.

Regarding claim 4, Kweon et al. discloses in Fig. 2A a semiconductor device, comprising:

- a semiconductor chip (21);
- a lead frame (23, 25 and 27) which is provided with the semiconductor chip mounted thereon and electrically connected with the semiconductor chip; and
- a printed circuit board (28) including conductive pads (29), which are formed thereon and brought into direct contact with a bottom surface of the lead frame.

Kweon et al. does not disclose the uneven roughness existing on the bottom surface of the lead frame and a surface of the conductive pads. However, Takada et al. teaches in Fig. 3B an uneven roughness (22 and 23) existing on a bottom surface of a lead frame (50) and a surface of conductive pads (20). It would have been obvious to one of ordinary skill in the art at the time of the present invention was made to use the uneven rough contact surfaces of Takada et al. in the device of Kweon et al. in order to ensure stable contact between the external terminals of an electronic device and contact terminals as taught by Takada et al. in column 2, lines 40 ~ 44.

Regarding claim 18, Kweon et al., as modified, discloses in Fig. 2A a lead frame (23, 25 and 27) comprising a lead (25 and 27), said lead comprising an inner lead portion (25) connected

to an outer lead portion (27), said outer lead portion comprising the uneven roughness (22 and 23 of Takada et al.).

Regarding claim 19, Kweon et al., as modified, discloses in Fig. 2A ~ 2C the uneven roughness existing on contact surfaces between a pad (29) of said printed circuit board (28) and an outer lead (27) of said lead frame (23, 25 and 27).

Regarding claim 22, Kweon et al. discloses in Fig. 2A ~ 2C said lead frame comprising a lead, said lead comprising said bottom surface.

9. Claims 20 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art of Fig. 1 in view of Hashimoto.

The acknowledged prior art discloses in Fig. 1 a semiconductor device, comprising:

- a semiconductor chip (100);
- a chip-mounting substrate (103) which is provided with said semiconductor chip mounted on a top surface thereof and first conductive pads (107) formed on a bottom surface thereof and connected with said semiconductor chip electrically, said chip-mounting substrate including wirings (102);
- solder balls (106) formed on said first conductive pads;
- a printed circuit board (104) on which second conductive pads (108) connected with said solder balls are formed; and
- material injected (105) into a clearance formed between said chip-mounting substrate and said printed circuit board.

The acknowledged prior art does not disclose the wirings to be Cu and uneven roughness being formed on a contact surface between said Cu wirings of said chip-mounting substrate and said solder balls, and the uneven roughness existing on a bottom surface of the Cu wirings, and said Cu wirings are directly connected to the solder balls to form a joined surface. However, Hashimoto discloses in Fig. 2, Fig. 11A and column 8, lines 42 ~ 43 wirings to be Cu (46) and uneven roughness being formed on a contact surface between said Cu wirings (46) of a chip-mounting substrate (36) and solder balls (40), and the uneven roughness existing on a bottom surface of the Cu wirings, and said Cu wirings are directly connected to the solder balls to form a joined surface. It would have been obvious to one of ordinary skill in the art at the time of the present invention was made to use the uneven rough contact surface of Hashimoto in the device of the acknowledged prior art of Fig. 1 in order to increase a contact area as taught by Hashimoto.

Regarding claim 23, Hashimoto discloses in Fig. 2 and Fig. 11A said uneven roughness being continuously formed on said bottom surface of said Cu wiring.

Response to Arguments

10. Applicant's arguments with respect to claims 1, 4 and 20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
July 24, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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